Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

Listing of Claims

Claims 1-18 (Cancelled)

19. (Previously Presented) An apparatus comprising:

a first printed circuit board;

a processor mounted to the first printed circuit board, wherein the processor comprises a development port;

a system bus formed on the first printed circuit board and coupled to the processor;

a second bus formed on the first printed circuit board and coupled to the development port.

20. (Previously Presented) The apparatus of claim 19 further comprising

a second printed circuit board;

a first data storage device mounted on the second printed circuit board, wherein the first data storage device stores boot-up code;

a coupler, coupling the first printed circuit board to the second printed circuit board, defining at least a first data communication path from said second printed circuit board to said first printed circuit board;

wherein the boot-up code can be transmitted from the first storage device, over the first communication path, said second bus, to said development port of the processor.

21. (Previously Presented) The apparatus of claim 20 wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.

22. (Previously Presented) The apparatus of claim 20 wherein the second printed circuit board is configured to download the boot-up code to the development port automatically, in response to a power up or a reset of the apparatus.

23. (Currently amended) The apparatus of claim 20 wherein the first printed circuit board ~~comprisies~~ **comprises** a DRAM coupled to a memory controller and wherein said boot-up code comprises configuration information for configuring the memory controller.

24. (Previously Presented) The apparatus of claim 23 wherein the DRAM is coupled to the system bus.

25. (Previously Presented) The apparatus of claim 19 wherein the second bus comprises a serial data bus.

26. (Previously Presented) A method of booting up a system, wherein the system comprises a motherboard coupled to daughterboard, wherein the daughterboard comprises a microprocessor, a system bus, and a second bus, wherein the microprocessor is coupled to the system bus and the second bus, wherein the microprocessor comprises a development port coupled to the second bus, the method comprising:

transmitting a first boot-up code from said motherboard to said development port via the second bus, in response to a power-on or reset of said system; and

using said boot-up code, in said microprocessor to perform a first boot-up operation.

27. (Previously Presented) The method of claim 26 wherein said boot-up operation comprises configuring a port of the microprocessor that is different from said development port.

28. (Previously Presented) The method of claim 26 wherein said daughterboard comprises a DRAM and a memory controller, and wherein said boot-up operation comprises configuring said memory controller.

29. (Previously Presented) The method of claim 26 wherein said daughterboard comprises a DRAM coupled to the system bus, and wherein the method further comprises transmitting data from the mother board to the DRAM via the system bus.

30. (Previously Presented) The method of claim 29 wherein the data comprises an operating system for said microprocessor.

31. (Previously Presented) An apparatus comprising:

a first printed circuit board coupled to a second printed circuit board;

a processor mounted to the first printed circuit board, wherein the processor comprises a development port;

a system bus coupled to the processor;

a second bus coupled to the development port, wherein the second bus is formed on the first printed circuit board;

means for downloading a boot-up code from said second printed circuit board to said development port via the second bus, in response to a power on or reset of said apparatus.

32. (Previously Presented) The apparatus of claim 31 wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.